REMARKS

Claims 2-4 remain in the application for consideration of the Examiner with Claim 1 standing cancelled.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Claim 2 was rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written requirement.

The Examiner alleges that the equation found in Claim 2 fails to be adequately defined and therefore described in the specification.

The Examiner's attention is directed to page 7, line 27. Here this equation is presented.

It is respectfully submitted that Claim 2 is in full compliance with 35 U.S.C. § 112, first paragraph.

Claims 3 and 4 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

This rejection is respectfully traversed.

The Examiner alleges that it is not clear what "for plating-electricity-supply-use" conductor pattern means.

However, the Examiner's attention is directed to page 9, line 13, et seq. where this aspect is discussed and consequently defined.

Turning now to the art rejections, Claims 1 and 2 were rejected under 35 U.S.C. § 102(a) as being anticipated by Kondou; Claims 1-4 were rejected under 35 U.S.C. § 102(a) as being anticipated by Distefano; and Claims 1-4 were rejected under 35 U.S.C. § 102(a) as being anticipated by Amagai.

These rejections are respectfully traversed.

The reference to Kondou is not applied to Claims 3 and 4.

Distefano does not disclose or suggest the presently claimed invention including the for plating electrical supply use conductor pattern electrically connected with the plurality of circuit patterns in now independent Claim 3.

The Examiner alleges that Distefano discloses a plurality of circuit patterns 108.

However, notwithstanding the allegations of the Examiner, these are not for plating electrically supply use conductor patterns.

Amagai does not disclose or suggest the presently claimed invention including the for plating electrically supply use conductor pattern upon the electrically connected with the plurality of circuit pattern.

The Examiner alleges that 7A are circuit patterns.

However the circuit patterns alleged by the Examiner are not seen in conjunction with the sprocket holes.

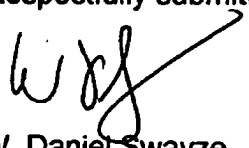
More particularly, Figures 5 and 6 do not show the for plating electrically supply use conductor pattern electrically connected with the plurality of circuit patterns.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



W. Daniel Swayze, Jr.
Attorney for Applicant
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633